# Synchronizing multiple E1430A modules

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There was a certain difficulty to synchronize ADC clocks of several HP E1430A modules. They were installed in a E8401A crate with a NI VXI-MXI-2 extender module in Slot 0. The digitizer modules were next to each other with the master being the leftmost. A group was created in the software and synchronization was setup along the explanation in the E1430A user manual and the available software samples. During data taking it turned out that ADC clocks were synchronous, but sometime one or two of the four modules had lost a cycle or a fraction of a cycle. This could be demonstrated by sampling a 0.8 Vss 102.4 kHz sine wave at 10.24 MSamples/sec, triggering at 0.1 V.
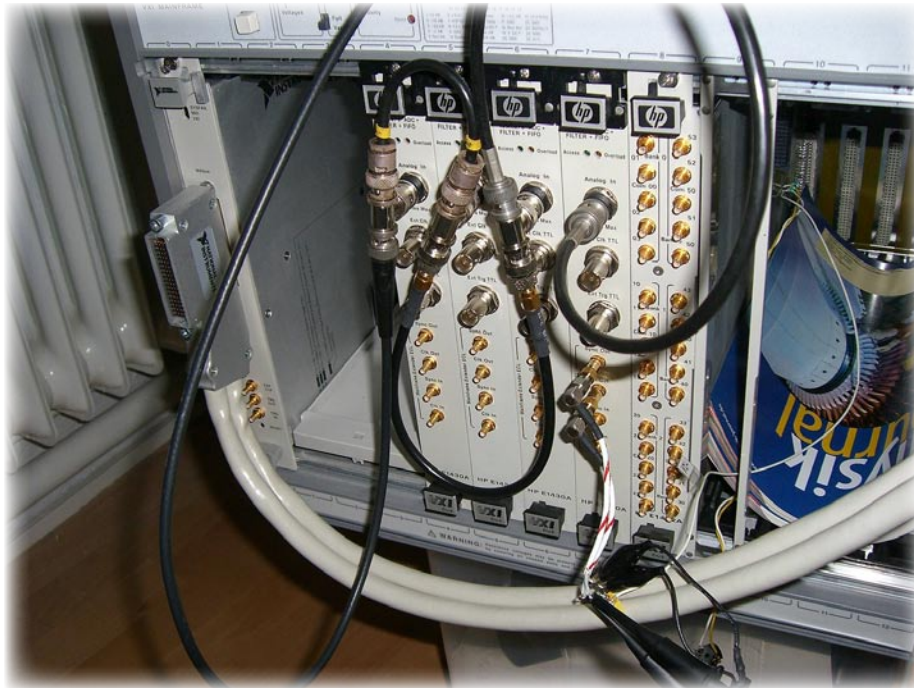
VXI crate with extender and group of digitizers. An empty and half open E1407C is used as a breakout box. Empty slots are ventilation blocked.

First i tried to understand how synchronization was supposed to work. Somehow i assumed that the VXI Clk10 backplane clock distribution was being used, and that eventually signals injected by the extender and the master module at the same time could cause problems. I was wondering if there was a way of making the master module drive the sync line but not the clock line.

The HP user manual isn't clear about that logic. For example they don't explain how we have a SMB clock in and a BNC clock in and only one of them is called external clock. They also don't explain that a module in multisync state receives its clock from the bus and that this state does not affect the sync signal logic. Only the software driver manages sync generation by one "master" module in the group and sync receipt by the other "slave" modules in the group.

When you open the E1430A and look inside, you find that the Clk10 lines are not connected at all. Instead these HP modules use ECLTRIG0 for sync and ECLTRIG1 for clock. The bus interface is made of two MC10H116 triple line drivers, a MC10E116 quint line driver and a MC10H123 triple bus driver, plus some pulldown resistor array and the two 150 Ohm resistors recommended in the VXI specification.

After two line driver delays the state of each two VXI bus lines appears on the E1430A front panel SMBs labeled "Sync Out" and "Clk Out". Note: In order to view these ECL signals with a scope, you have to connect some pulldown loads.
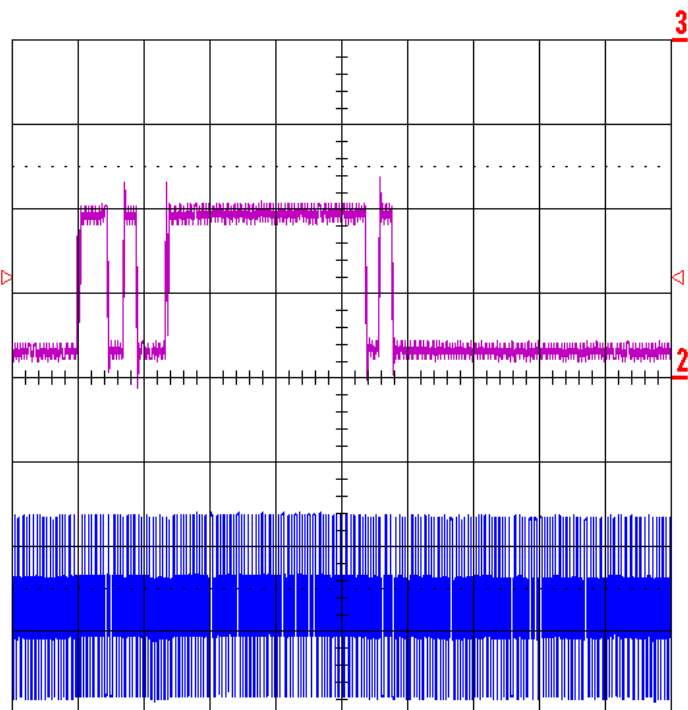
The two ECL lines connected to -2 V$_{CC}$ via 50 Ohm pulldowns and to the scope probes.

Sync and clock during e1430_reset_dsp().

The signals looked clean, except that during synchronization there are 5 nsec low glitches in the pulled sync signal, always precisely 0.75 µsec after sync line pulled by master. Anyway, these glitches don't matter, since the sync signal is sampled at the rising edge of the clock signal. The clock signal appears as a short positive pulse (asymmetric).
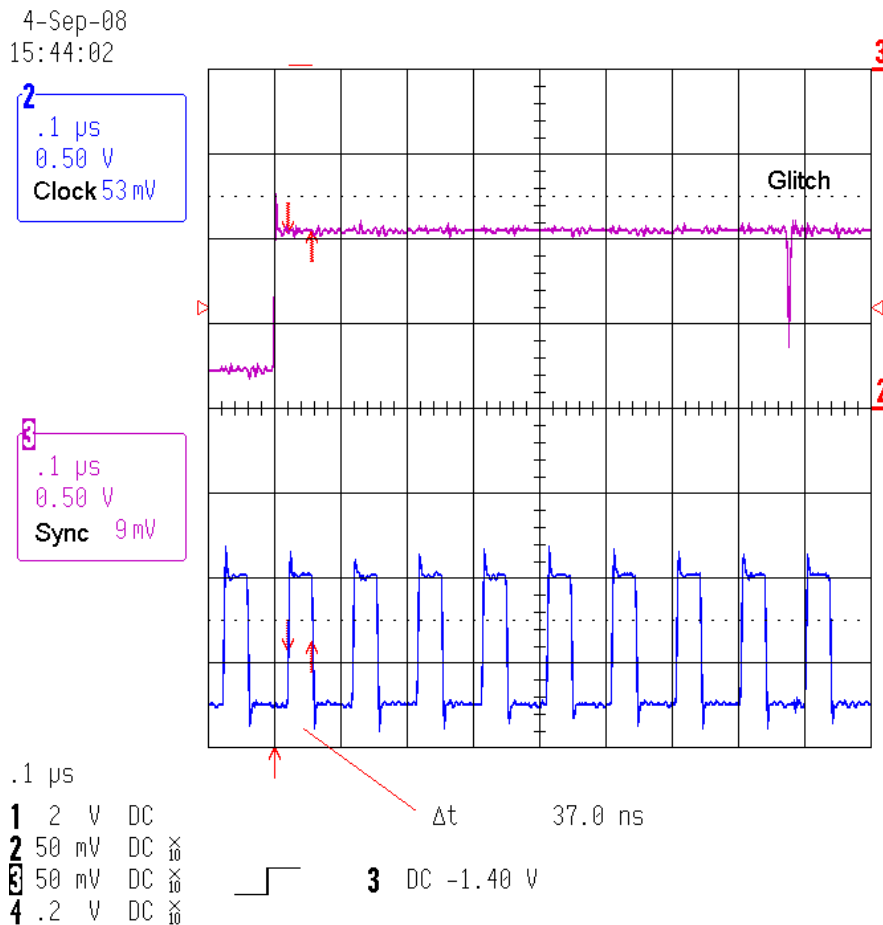
Sync and clock detail with glitch mentioned in text.

The "Clk In" front panel SMB drives the backplane ECLTRIG1 line via a wired OR connection, unconditionally as far as i understand.

Obviously every E1430A has the built-in capability to be a VXI crate clock driver for its slaves. The VXI Clk10 design isn't a bus but a fan out, and it's input is always from Slot 0 - the vxi crate controller/extender. This is the reason for using the ECLTRIG1 bus when clocking the slaves. The bus causes some nsec propagation delays but the effect is known and can be corrected during data analysis. As far as i have seen, the E1430A does not have a provision to receive its ADC clock from the Clk10 line. That would be a minor hardware change. The VXI specs do not require the Clk10 distribution to be propagation delay correct. It allows for a bus line with buffers, with 8 nsec maximum clock skew. I did not yet check whether the HP E8401A crate has such propagation delays.

So far i could not discover anything wrong. But the problem was found during the tests - just by luck.

It turned out i had a software problem. The group synchronization got spoiled by some E1430A API calls made later in the sequence that included autozero() and autorange(). As soon as i called e1430_reset_dsp() immediately before arming the group by e1430_arm_module(), everything worked fine. There was still some minor phase shift caused by the backplane clock propagation delays and the simple front panel signal distribution, but this was obvious.

ToDo

a) Refactor the driver software into some C++ classes. The HP software is messy, the manual full of little notes, hints and warnings. Interface should be much more abstract and more reliable to use.

b) Check the Clk10 propagation delays of the HP E8401A crate.

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